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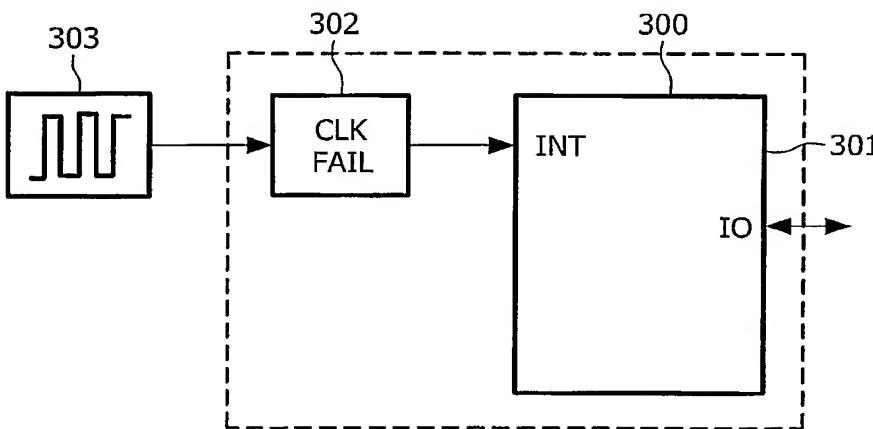
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(54) Title: ELECTRONIC CIRCUIT ARRANGEMENT FOR DETECTING A FAILING CLOCK



(57) Abstract: The invention relates to an electronic circuit arrangement (300) comprising a clock fail circuit (302) arranged for receiving a clock signal generated by a clock generation circuit (303) and generating an error signal upon the absence of the clock signal. The electronic circuit arrangement (300) further comprises an asynchronous processor (301) arranged for receiving said error signal on an interrupt input INT and to bring the electronic circuit arrangement in a pre-defined state upon detection of the error signal at the interrupt input INT by executing an interrupt routine.